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Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS



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MASSACHUSETTS INSTITUTE OF TECHNOLOGY LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 AUGUST — 31 OCTOBER 1992

26 FEBRUARY 1993

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 1992. The topics covered are Electrooptical Devices, Quantum Electronics, Materials Research, Submicrometer Technology, High Speed Electronics, Microelectronics, and Analog Device Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, DARPA, Navy, SDIO, and NASA.

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INTRODUCTION

1. ELECTROOPTICAL DEVICES

High CW power at 980 nm has been demonstrated from amplifiers and oscillators with tapered gain regions. Outputs as high as 3.0 W from an amplifier and 4.2 W from an oscillator have been achieved.

An analytical model has been developed for imperfections in mass-transported microlenses caused by inaccuracies in the original multistep mesa fabrication. Wavefront deformation and power loss have been evaluated and tolerable imperfections deduced for practical effort-saving fabrication of high-performance microoptical elements.

A monolithic two-dimensional array of surface-emitting AlGaAs diode lasers with dry-etched vertical facets and parabolic deflecting mirrors has been mounted on a W/Cu microchannel heatsink. Measurements indicate that CW output power densities as high as 148 W/cm² are possible with this type of array.

2. QUANTUM ELECTRONICS

A composite-cavity microchip laser has been constructed that tunes up to 30 GHz. The laser incorporates a LiTaO₃ electrooptic tuning element with acoustic damping to provide linear voltage-to-frequency conversion with a tuning sensitivity of 12 MHz/V at excursion rates from dc to several gigahertz.

3. MATERIALS RESEARCH

Undoped GaSb layers with a reproducibly low background acceptor concentration ($\sim 1 \times 10^{16}$ cm⁻³) have been grown by molecular beam epitaxy on (110) GaAs and GaSb substrates. By doping with Te donors provided by a GaTe source, n-GaSb layers have been grown with Hall mobilities as high as 7600 and 12 600 cm²/V s at room temperature and 77 K, respectively, which are about 50% greater than the highest reported values for n-GaSb epilayers grown on similar substrates.

4. SUBMICROMETER TECHNOLOGY

Several etching tools have been evaluated for the oxygen-based plasma pattern-transfer step in surface imaging and multilayer resist processes. These tools include a conventional parallel-plate reactive ion etcher, a magnetically enhanced reactive ion etcher, an electron cyclotron resonance reactor, and an RF helical resonator reactor.

Prototype vertical MOSFET devices using $2-\mu m$ geometries have been successfully fabricated. Such devices are being developed for implementing an ultradense transistor array for read-only memory and programmable read-only memory applications.

5. HIGH SPEED ELECTRONICS

A high-resolution transmission electron microscope has been used to study the structure of the tips of molybdenum field-emission cones. This work has shown that the tips have irregular protrusions with a typical radius of 1 nm and are covered by an amorphous native-oxide layer < 1 nm thick.

6. MICROELECTRONICS

An approximate method of calculating charge-transfer inefficiency as a function of packet size has been applied to a charge-coupled device having a special implant profile to harden it against bulk displacement damage. The calculations show good agreement with previously reported experimental data.

7. ANALOG DEVICE TECHNOLOGY

A 9-bit shift register has been fabricated that uses the new technology of single-flux-quantum logic. The circuit has been successfully demonstrated at clock frequencies up to 10 MHz.

REPORTS ON SOLID STATE RESEARCH

1 AUGUST THROUGH 31 OCTOBER 1992

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A High-Flux Atomic Oxygen Source for the Deposition of High T_c Superconducting Films	L. S. Yu-Jahnes W. T. Brogan A. C. Anderson M. J. Cima*	Rev. Sci. Instrum. 63 , 4149 (1992)
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Methacrylate Terpolymer Approach in the Design of a Family of Chemically Amplified Positive Resists	R. D. Allen* G. M. Wallraff* W. D. Hinsberg* L. L. Simpson* R. R. Kunz	In Polymeric Materials Science and Engineering, ACS Symposium Series (American Chemical Society, Washington, D.C.)
Photonic-Crystal Planar Antennas	E. R. Brown	Opt. Photon. News
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MBE Growth of SHOC Lasers Using the InGaAs/AlGaAs Materials System	W. D. Goodhue H. Q. Le S. DiCecca	J. Vac. Sci. Technol. B
Quantum-Well GaAs/AlGaAs Shallow- Donor Far-Infrared Photoconductors Grown by MBE	W. D. Goodhue E. R. Mueller* D. M. Larsen* J. Waldman* Y. H. Chai* S. C. Lai* G. D. Johnson	J. Vac. Sci. Technol. B

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Modeling of Resist Performance	M. A. Hartney	Adv. Mater. Opt. Electron.
Modeling of Positive-Tone Silylation Processes for 193-nm Lithography	M. A. Hartney	J. Vac. Sci. Technol. B
Surface Imaging Resists for 193-nm Lithography	D. W. Johnson* M. A. Hartney	Jpn. J. Appl. Phys.
Wet-Developed Bilayer Resists for 193-nm Excimer Laser Lithography	R. R. Kunz M. W. Horn P. A. Bianconi* D. A. Smith* J. R. Eshelman*	J. Vac. Sci. Technol. B
Surface-Imaged Silicon Polymers for 193-nm Excimer Laser Lithography	R. R. Kunz M. W. Horn R. B. Goodman G. M. Wallraff* R. D. Miller* E. J. Ginsberg* P. A. Bianconi* D. A. Smith* J. R. Eshelman*	Jpn. J. Appl. Phys.
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Photolithography at 193 nm and Below	M. Rothschild	J. Vac. Sci. Technol. B

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PRESENTATIONS†

Monolithic Two-Dimensional Surface-Emitting Horizontal-Cavity Diode-Laser Arrays with up to 66% Differential Quantum Efficiencies	W. D. Goodhue J. P. Donnelly C. A. Wang R. J. Bailey G. A. Lincoln G. D. Johnson	Summer Topical Meeting on Integrated Optoelectronics, Santa Barbara, California, 5-7 August 1992
Single-Flux-Quantum Shift Register	K. A. Delin	NATO Advanced Study Institute on the New Superconducting Electronics,
A High-Speed Superconducting Analog Sampler	J. Przybysz* J. P. Sage	Waterville Valley, New Hampshire, 9-20 August 1992
The Monolithic Optoelectronic Transistor (MOET)	B. A. Aull E. R. Brown P. A. Maki C. Mehanian K. B. Nichols S. C. Palmateer	LEOS Topical Meeting on Smart Pixels, Santa Barbara, California, 10-12 August 1992
Strong Normal-Incidence Intersubband Absorption in <i>n</i> -type Ellipsoidal- Valley Quantum Wells	S. J. Eglash E. R. Brown K. A. McIntosh	1992 Meeting of the IRIS Specialty Group on Infrared Detectors, Moffett Field, California, 10-14 August 1992
Vertical Gradient-Freeze Growth of Aluminate Crystals	R. E. Fahey A. J. Strauss A. C. Anderson	10th International Conference on Crystal Growth, San Diego, California, 16-21 August 1992
Radiative Renormalization Analysis of Optical Double Resonance	P. L. Kelley O. Blum* T. K. Gustafson*	Optical Society of America Meeting on Nonlinear Optics: Materials, Fundamentals, and Applications, Maui, Hawaii, 17-21 August 1992

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[†]Titles of presentations are listed for information only. No copies are available for distribution.

A Compact Solid State Laser for Generation of a Mesospheric Sodium Guide Star	T. H. Jeys K. F. Wall
The Use of Single-Surface Superconducting Resonators to Measure Low-Temperature Loss of Dielectric Films	M. Bhushan R. M. Lerner M. W. Horn J. S. Logan* K. Stein*
High Temperature Superconducting Films on Thinned Dielectrics for High Density Microwave Circuits	S. M. Garrison* GC. Liang* B. F. Cole* N. Newman* R. S. Withers* A. C. Anderson
Experimental Results on a Scanned-Beam Microstrip Antenna Array with a Proximity-Coupled YBCO Feed Network	J. S. Herd* D. Hayes* J. P. Kenney* L. D. Poles* K. G. Herd* W. G. Lyons
Modeling the Nonlinear Resistance of Superconducting Striplines	C. W. Lam* S. M. Ali* D. E. Oates
Analysis of Superconducting Transmission- Line Structures for Passive Microwave Device Applications	L. H. Lee* S. M. Ali* W. G. Lyons

Optical Society of America Topical Meeting on Adaptive Optics for Large Telescopes, Maui, Hawaii, 17-21 August 1992

1992 Applied Superconductivity Conference, Chicago, Illinois, 24-28 August 1992

D. E. Oates J. D. Goettee*

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High-Temperature Superconducting		
Delay Lines and Filters on Sapphire		
and Thinned LaAlO ₃ Substrates		

G.-C. Liang* R. S. Withers* B. F. Cole* S. M. Garrison* M. E. Johansson*

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Implementation of a YBa₂Cu₃O_{7-x} Wideband Real-Time Spectrum-Analysis Receiver

W. G. Lyons D. R. Arsenault M. M. Seaver R. R. Boisvert T. C. L. G. Sollner R. S. Withers

Nonlinear Surface Resistance in YBa₂Cu₃O_{7-x} Thin Films

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Design, Fabrication, and Testing of a High-Speed Analog Sampler

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Microwave Measurements of YBCO, Nb, and NbN Thin Films in the Mixed State

J. Steinbeck* D. E. Oates A. C. Anderson

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Electrical Properties of MBE Grown Layers of AlGaAsSb and the Effects of Proton Implantation and Hydrogen Plasma Treatment

S. J. Eglash M. Ye* S. J. Pearton* R. G. Wilson* 7th International Conference on Molecular Beam Epitaxy, Schwäbisch Gmünd, Germany, 24-28 August 1992

1992 Applied Superconductivity

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Chicago, Illinois,

24-28 August 1992

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Optical Modulators for Analog Link Applications	G. E. Betts L. M. Johnson C. H. Cox III	
Development of GaInAsP/GaAs Strained-Layer Quantum-Well Diode Lasers	S. H. Groves Z. L. Liau S. C. Palmateer J. N. Walpole L. J. Missaggia	
Interferometric Modulators for an Adaptive Nulling System	L. M. Johnson H. V. Roussell G. E. Betts	SPIE's OE/Fibers '92, Boston, Massachusetts, 8-11 September 1992
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Diamond Transistors	M. W. Geis	20th Annual Symposium of the Rocky Mountain Chapter of the American Vacuum Society, Denver, Colorado, 10 September 1992
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PbTeSe/BiSb Short-Period Superlattice as a New Thermoelectric Cooling Material	T. C. Harman	Workshop on Thermoelectric Devices, Ft. Belvoir, Virginia, 17 September 1992

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Optical Materials for Deep-UV Lithography	M. Rothschild	20-25 September 1992
Laser Induced Microfabrication Technologies	D. J. Ehrlich	National Optics Institute, Quebec, Canada, 9 October 1992
MBE Growth of SHOC Lasers Using the InGaAs/AlGaAs Materials System	W. D. Goodhue H. Q. Le S. DiCecca	
Quantum-Well GaAs/AlGaAs Shallow- Donor Far-Infrared Photoconductors Grown by MBE	W. D. Goodhue E. R. Mueller* D. M. Larsen* J. Waldman* Y. H. Chai* S. C. Lai* G. D. Johnson	North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, 12-14 October 1992
MBE Growth of High-Mobility n-GaAs	G. W. Turner S. J. Eglash A. J. Strauss	
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The Lincoln Laboratory 193-nm Program—Status Update	M. Rothschild	Sematech Workshop on DUV, Austin, Texas, 26-27 October 1992
Excimer-Laser Induced Degradation in Bulk Fused Silica	M. Rothschild J. H. C. Sedlacek	24th Symposium on Optical Materials for High Power Lasers, Boulder, Colorado, 28-30 October 1992
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QUANTUM ELECTRONICS

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HIGH SPEED ELECTRONICS

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1. ELECTROOPTICAL DEVICES

1.1 HIGH-POWER TAPERED SEMICONDUCTOR AMPLIFIERS AND OSCILLATORS AT 980 nm

Semiconductor devices with tapered gain regions have been demonstrated to produce a high-power nearly diffraction-limited beam with good efficiency at 980 nm. Over 1 W of output power from tapered amplifiers [1],[2] and tapered oscillators operating as unstable resonators [3] has been achieved previously. Here, we report nearly diffraction-limited CW output power as high as 3.5 W from a tapered amplifier and as high as 4.2 W from a tapered oscillator.

Figure 1-1 shows a schematic top view of the tapered device structure. The devices are fabricated from single-quantum-well strained-layer InGaAs/AlGaAs graded-index separate-confinement heterostructure (GRINSCH) material. The tapered gain region is defined by a metallized electrical contact pad. The angle of the taper is designed to accommodate the diffraction of a beam propagating from the narrow end of the taper. Perpendicular to the junction, the light is confined in the single-mode GRINSCH waveguide. Etched grooves on either side of the narrow end of the taper raise the threshold for lasing in the case of the amplifier and act as a mode-selective filter in the case of the oscillator. The devices are cleaved to lengths ranging from 2 to 3 mm and have output apertures ranging from 215 to 325 μ m. The amplifiers and oscillators differ only in the reflectivity of the facet coatings. An amplifier has both facets antireflection coated ($R_1 = R_2 \approx 1\%$), while an oscillator has the output facet antireflection coated and the back facet left uncoated ($R_1 \approx 30\%$). The oscillator spatial mode is established self-consistently, as described by Fox and Li [4] for lossy cavities with various mirror configurations.

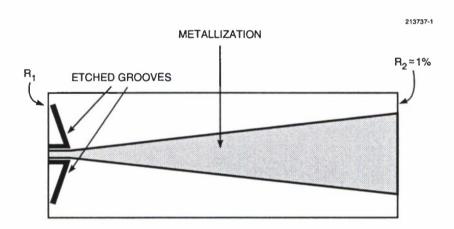


Figure 1-1. Schematic of the tapered amplifier or oscillator. R_1 is ~ 1% for the amplifier and ~ 30% for the oscillator.

The 3.5-W output power from a 2-mm-long amplifier was achieved at a bias current of 5.0 A and with 90 mW of optical input power incident on the input focusing lens. The far-field intensity profile in the plane parallel to the junction is shown in Figure 1-2, where the quadratic curvature of the diverging wavefront has been removed. The central lobe contains 89% of the total power (3.1 W) and has a width of 0.24° full width at half-maximum (FWHM), which is ~ 1.05 times the diffraction limit for the $215-\mu m$ aperture.

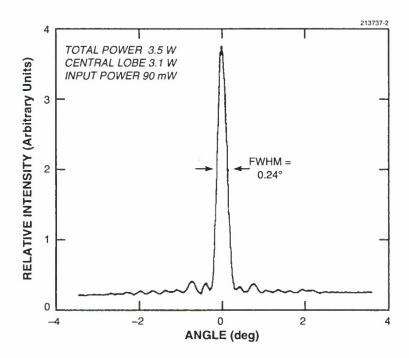


Figure 1-2. Far-field beam profile of the 3.5-W amplifier output.

The 4.2-W output power from a 3-mm-long oscillator was achieved at a bias current of 10 A, as shown in Figure 1-3. The far-field profile measured at 9.0 A (Figure 1-3 inset) shows that the beam is predominantly single lobed with a width of 0.26° FWHM (1.7 times the diffraction limit for a $325-\mu m$ aperture). Above 10.5 A, catastrophic optical damage occurred to the uncoated back facet.

Many applications of the tapered amplifiers and oscillators require either collimating the output into a low-aberration free-space beam with a circular cross section, or efficient coupling of the output into a single-mode optical fiber. In either case, transformation of the beam is complicated by two features resulting from the tapered gain region, namely, large astigmatism and an aspect ratio that differs from unity. Preliminary attempts to couple the 2.6-W output power of a 2-mm-long oscillator into a single-mode fiber have led to achievement of 400 mW of power into the fiber with a net fiber-coupling

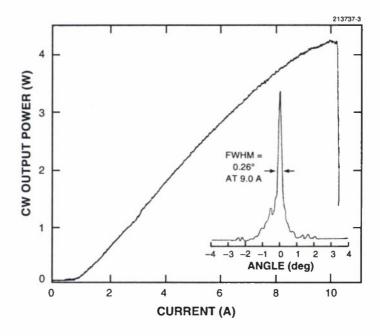


Figure 1-3. Output power vs current for the tapered oscillator. The inset shows the far-field profile at 9.0 A.

efficiency of 20%. This efficiency is consistent with the value expected from measurement of the beam quality and the optics used. While 400 mW is a significant achievement for power into a single-mode fiber from a semiconductor device, we believe that further optimization of the coupling optics can lead to coupling efficiencies closer to 40% for oscillators, and even greater for tapered amplifiers since they have superior beam quality.

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1.2 TOLERANCES IN MICROLENS FABRICATION BY MULTILEVEL ETCHING AND MASS-TRANSPORT SMOOTHING

Microlenses fabricated by mass-transport smoothing of multilevel mesa structures in semiconductor substrates have high indices and accurate profiles, making them potentially well suited for large-numerical-aperture microoptical applications and monolithic optoelectronic integration [5]. However, the quest for very high degrees of accuracy in the lithographic definition of the multilevel structure can become rather time-consuming. In this work, an analytical model has been developed for the lens imperfections, and tolerable inaccuracies have been deduced that would permit practical, time-saving fabrication.

Lithographic inaccuracy in the form of a small misalignment in one of the mesa steps is illustrated in Figure 1-4(a). The misalignment, in effect, introduces an incremental mass (positive or negative) along the step edges, which then becomes a small hump or a shallow depression in the smoothed lens [Figure 1-4(b)]. Detailed profiles of these imperfections [Figure 1-4(c)] and their influence on the lens performance are treated quantitatively in the following analysis.

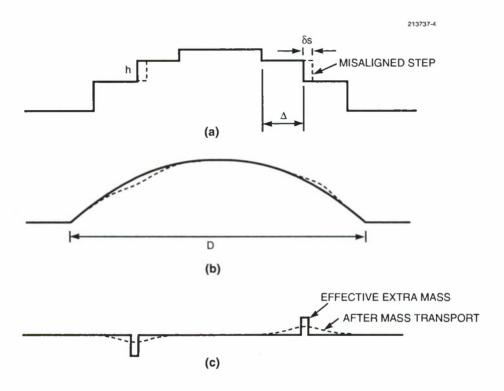


Figure 1-4. Illustrations of (a) a misaligned mesa step, (b) the resulting hump and depression in an otherwise ideal lens after mass-transport smoothing, and (c) the net lens distortions that can be used in the calculation of wavefront deformation and light scattering.

The effective width of the hump (or depression) is expected to be approximately the step width Δ , since that is the extent of mass transport needed for a totally smoothed lens. In the case of cylindrical lenses, the detailed profile of the hump can be quantitatively treated by using previously developed mass-transport models, in which the evolution of a surface profile is described by the exponential decay of its Fourier components [6]–[9]. The initial profile height δz of the hump can be approximated by

$$\delta z(x,0) \approx \delta A \ \delta(x) = \frac{\delta A}{\pi} \int_{0}^{\infty} \cos kx \, dk \ ,$$
 (1.1)

where $\delta A = h \, \delta s$ is the cross-sectional area of the hump, as shown in Figure 1-4, k is the wave number of the Fourier component, and the spatial origin is taken at the center of the hump for convenience. Then, the profile height at time t becomes

$$\delta z(x,t) = \frac{\delta A}{\pi} \int_{0}^{\infty} e^{-\gamma t k^{4}} \cos kx \, dk \quad , \tag{1.2}$$

where γ is the mass-transport coefficient [9]. By defining

$$\xi = x/(\gamma t)^{1/4} \tag{1.3}$$

and

$$\kappa \equiv k(\gamma t)^{1/4} \quad , \tag{1.4}$$

Equation (1.2) becomes

$$\delta z(x,t) = \frac{\delta A}{\pi (\gamma t)^{1/4}} \int_{0}^{\infty} e^{-\kappa^4} \cos \kappa \xi \, d\kappa \quad . \tag{1.5}$$

Note that the integral is a function of ξ only. The profile thus maintains the same functional form but is laterally inflated and vertically deflated according to $(\gamma t)^{1/4}$.

The mass-transport time t needed to complete the lens formation is such that the grading of each mesa step equals the step width Δ . The grading has previously been analyzed and is given by the mass-transport length L, whose relationship with γt has been derived [9]. Using that relationship, we have

$$\left(\gamma t\right)^{1/4} = \frac{\Gamma(1/4)\Delta}{4\pi} \ . \tag{1.6}$$

By substituting Equation (1.6) into Equation (1.5), we have at the completion of the lens formation

$$\delta z(x) = \frac{4\delta A}{\Gamma(1/4)\Delta} \int_{0}^{\infty} e^{-\kappa^4} \cos \kappa \xi \, d\kappa , \qquad (1.7)$$

with

$$\xi = \frac{4\pi x}{\Gamma(1/4)\Delta} \ . \tag{1.8}$$

The integral in Equation (1.7) can be evaluated by using the series expansion of $\cos \kappa \xi$, i.e.,

$$\int_{0}^{\infty} e^{-\kappa^{4}} \cos \kappa \xi \, d\kappa = \int_{0}^{\infty} e^{-\kappa^{4}} \sum_{n=0}^{\infty} (-1)^{n} \, \frac{\left(\kappa \xi\right)^{2n}}{(2n)!} \, d\kappa$$

$$= \sum_{n=0}^{\infty} \frac{(-1)^{n} \, \xi^{2n}}{(2n)!} \, \int_{0}^{\infty} \kappa^{2n} e^{-\kappa^{4}} \, d\kappa . \tag{1.9}$$

The last integral in Equation (1.9) can readily be identified as the gamma function by using the change of variable $u = \kappa^4$, i.e.,

$$\int_{0}^{\infty} \kappa^{2n} e^{-\kappa^{4}} d\kappa = \frac{1}{4} \int_{0}^{\infty} u^{(n/2) + (1/4) - 1} e^{-u} du$$

$$= \frac{1}{4} \Gamma\left(\frac{2n+1}{4}\right). \tag{1.10}$$

Hence, Equation (1.7) becomes

$$\delta z(x) = \frac{\delta A}{\Delta} \sum_{n=0}^{\infty} (-1)^n \frac{\Gamma[(2n+1)/4]}{\Gamma(1/4)\Gamma(2n+1)} \, \xi^{2n} \quad . \tag{1.11}$$

This series is then evaluated by using properties and tabulated values of the gamma function [10], in particular $\Gamma(1/4) = 3.626$, $\Gamma(3/4) = 1.226$, $\Gamma(1) = 1$, and $\Gamma(a+1) = a\Gamma(a)$. The calculated $\delta z(x)$ is shown as solid squares in Figure 1-5.

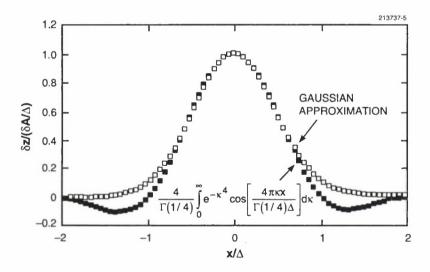


Figure 1-5. Calculated profile of an extra mass after mass-transport smoothing and its comparison with a Gaussian profile of the same height and width. The scaling parameter Δ is the original mesa step width, and δA is the cross-sectional area of the extra mass.

Note that $\delta z(x)$ has a maximum value of exactly $\delta A/\Delta$ and a full width at half-maximum of $\Gamma(1/4)\Delta/\pi$, or 1.15 Δ . For practical purposes, the profile can be approximated by a Gaussian one with the same height and width,

$$\delta z(x) \approx \frac{\delta A}{\Delta} e^{-x^2/\left[(2/3)\Delta\right]^2}$$
, (1.12)

shown as the open squares in Figure 1-5. This approximation yields mean-square wavefront deformation (see below) to within a few percent of the exact one.

Power loss, or decrease in intensity I, in the collimated beam is then given by [11]

$$\frac{\delta I}{I} = \frac{\int_{-D/2}^{D/2} \left[2\pi (n-1)\delta z/\lambda \right]^2 E(x') dx'}{\int_{-D/2}^{D/2} E(x') dx'},$$
(1.13)

where D is the lens aperture, n is the refractive index of the lens material, λ is the wavelength in vacuum, and E(x') is the light amplitude across the aperture (with the origin of x' located at the lens center). For a uniformly illuminated lens, Equation (1.13) becomes

$$\frac{2\int\limits_{I}^{\infty} \left[2\pi(n-1)\delta_{Z}/\lambda\right]^{2} dx}{D},$$
(1.14)

where the $\pm \infty$ integration limits are justified by $\Delta \ll D$ and the factor of 2 reflects an equal contribution from the depression. By substituting Equation (1.12) into Equation (1.14) and carrying out the integration, we obtain

$$\frac{\delta I}{I} \approx \frac{(5/6) \left[2\pi (n-1)(\delta A/\Delta)/\lambda \right]^2}{N} , \qquad (1.15)$$

where $N \equiv (1/2)(D/\Delta)$ is the number of etched steps.

Equation (1.15) can be conveniently used to estimate the power loss from measured δA . In practical fabrications, mesa misalignment $\delta s < 0.5 \ \mu m$ can be routinely achieved. This corresponds to $dA \le 0.5 \ \mu m^2$ for average step height $h = 1 \ \mu m$. For a step width $\Delta = 15 \ \mu m$, the overall height of the resulting hump, $\delta A/\Delta$, is 0.033 μm . Equation (1.15) then yields $\delta I/I \le 3.5\%$ for $\lambda = 1 \ \mu m$, n = 3.2, and N = 5.

The loss due to a single < 0.5- μ m misalignment is thus relatively small. When several random misalignments are present, the total loss is given by the sum of individual ones. The summation needs to be weighed by the amplitude distribution for lenses not uniformly illuminated [cf. Equation (1.13)].

Other types of lithographic inaccuracies such as errors in step width or height can be treated in a similar way, and Equation (1.15) can be used as a good approximation.

In conclusion, a comprehensive model has been developed in which lithographic inaccuracies in mass-transport microlens fabrication are treated quantitatively. The resulting knowledge of acceptable imperfections is useful in practical applications of this promising microoptical technology.

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1.3 CW OPERATION OF MONOLITHIC ARRAYS OF SURFACE-EMITTING AlGaAs DIODE LASERS WITH DRY-ETCHED VERTICAL FACETS AND PARABOLIC DEFLECTING MIRRORS

The fabrication and pulsed operation of high-quantum-efficiency two-dimensional monolithic arrays of AlGaAs diode lasers with dry-etched vertical facets and parabolic deflecting mirrors [12] have been reported recently. The use of parabolic instead of straight 45° mirrors permits the fabrication of low f-number deflectors in a planar structure and in addition reduces the output beam divergence perpendicular to the junction plane from $\geq 36^{\circ}$ to $\sim 13^{\circ}$. Under both short-pulse and quasi-CW operation, these arrays had threshold current densities $J_{\rm th}$ of 220–240 A/cm², comparable to those of cleaved-facet broadarea lasers fabricated in the same material, and differential quantum efficiencies η_d as high as 66%. Here, we report the CW performance of an array of this type mounted on a W/Cu microchannel heatsink.

A schematic illustration of an array mounted on a heatsink is presented in Figure 1-6. The laser structure for the array used in these studies is GRINSCH single-quantum-well AlGaAs/GaAs grown on an n^+ -GaAs substrate by organometallic vapor phase epitaxy. The quantum well is 10 nm thick and contains about 7-mol% AlAs. Chlorine ion-beam-assisted etching (IBAE) was used to etch the facet and parabolic deflecting mirrors [13]. To achieve high-quality laser facets, 4:1 projection lithography was employed to define the photoresist etch mask used during the IBAE of the facets. For the deflector etch steps, the angle of the sample holder relative to the ion beam is stepped via computer control during the etch to achieve the desired concave shape [13]. Further details of the design and fabrication of the arrays can be found in [12].

For evaluation of these arrays under CW operating conditions, a 0.54-cm^2 array cleaved from a 1-cm^2 sample was soldered to a W/Cu microchannel heatsink using evaporated Au/Sn. The heatsink is $\sim 500~\mu\text{m}$ thick. A dicing saw was used to cut $100\text{-}\mu\text{m}$ -wide, $400\text{-}\mu\text{m}$ -deep microchannels on $200\text{-}\mu\text{m}$ centers. After the array was soldered to the heatsink, a Cu bus bar (not shown in Figure 1-6) was soldered to the top of each row. The Cu bars provide good electrical conductivity along the rows and also act as a heat spreader, evening out temperature variations along the top of the rows in this junction-side-up configuration. The mounted array was then soldered into a cooling module that contained the necessary cooling water and electrical connectors [14]. The near-field pattern of this array, which consists of 5 rows of 75 lasers each, is shown in Figure 1-7.

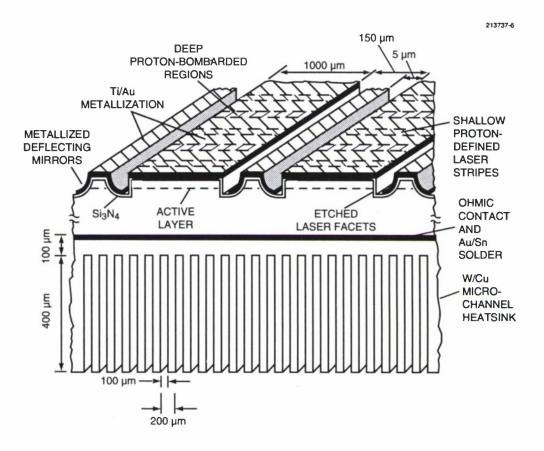


Figure 1-6. Schematic diagram of a monolithic surface-emitting array of AlGaAs diode lasers with dry-etched vertical facets and parabolic deflecting mirrors.

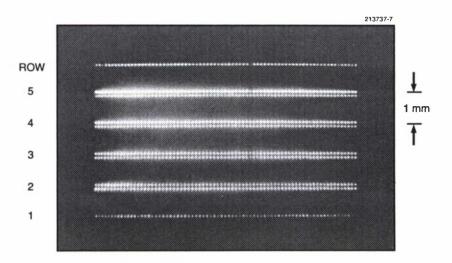


Figure 1-7. Near-field pattern of a 0.54-cm² array consisting of 5 rows of 75 elements each and operating at 504-nm wavelength.

The CW output power vs current of two sections of the array is shown in Figure 1-8. A section consisting of rows 1 through 4 ($\sim 0.43~\rm cm^2$) had a $J_{\rm th}$ of 240 A/cm² and an effective CW η_d of 46%. The current-limited output power of 37 W corresponds to a power density of 84 W/cm². Row 5 was driven separately and had a $J_{\rm th}$ of 240 A/cm² and an effective CW η_d of 48%. The output power at 28 A was 16 W, which corresponds to a power density of 148 W/cm².

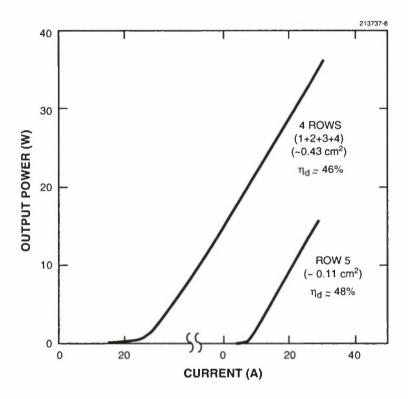


Figure 1-8. CW output power vs current of rows 1 to 4 ($\sim 0.43 \text{ cm}^2$) driven in parallel, and row 5 ($\sim 0.11 \text{ cm}^2$) driven separately.

The output spectra of row 5 under pulsed operation and at several different CW currents are shown in Figure 1-9. The spectrum obtained at 25 A CW compared to that obtained under pulsed conditions indicates an average temperature rise of about 22°C. This temperature rise is consistent with the efficiency of the array and with the calculated thermal resistance of the W/Cu microchannel heatsink [14],[15]. Since the thermal cross talk between the rows is small, the single-row measurement gives a good estimate (within 15%) of that expected in a full 1-cm² array.

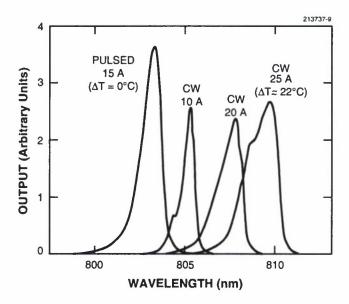


Figure 1-9. Output spectra for row 5 under pulsed operation and at several different CW currents.

These results indicate that low- $J_{\rm th}$, high- η_d monolithic arrays having CW power outputs on the order of 150 W/cm² with acceptable temperature rises are achievable. In addition, for applications that require high brightness, the reduced beam divergence of these arrays due to the use of parabolic deflecting mirrors should reduce the lenslet array requirements and improve alignment tolerances for obtaining acceptable collimation of the individual outputs.

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2. QUANTUM ELECTRONICS

2.1 DIODE-PUMPED COMPOSITE-CAVITY ELECTROOPTICALLY TUNED MICROCHIP LASER

Microchip lasers [1] have been frequency tuned using a variety of techniques including thermal tuning, piezoelectric tuning [2], and pump-diode modulation [3]. Each of these techniques provides frequency modulation at low excursion rates and has advantages for a given set of applications. However, for applications such as frequency-modulated optical communications and chirped coherent laser radar, extremely high rates of tuning are required. These rates can only be achieved electrooptically [4]. With composite-cavity electrooptically tuned microchip lasers, linear voltage-to-frequency conversion can be obtained with uniform, high-sensitivity tuning at modulation frequencies from dc to several gigahertz.

The frequency response of a laser whose optical length is varied is well understood. When a linear voltage ramp is applied to the electrooptic tuning element, the frequency of the laser undergoes a series of steps whose spacing in time is the cavity round-trip time t_r [5]. When the rise time T of the voltage is long compared to the cavity round-trip time, the frequency has an approximately linear chirp with a fractional deviation from linearity of t/2T. Hence, high-speed tuning is most linear when the shortest possible laser cavity is used. Since the free spectral range of a cavity increases with decreasing cavity length, the maximum excursion frequency of a laser is also obtained by using the shortest possible cavity.

The sensitivity of electrooptic voltage-to-frequency conversion increases linearly with the percentage of the cavity length filled with electrooptic material. For high-sensitivity tuning it is desirable to fill the cavity with as much of this material as possible. However, as the length of the electrooptic crystal is increased, the capacitance between its electrodes rises, resulting in higher energy requirements and slower electrical response. In addition, the linearity at high excursion rates decreases, and the maximum frequency excursion is reduced. For these reasons, the minimum-cavity-length configuration of the composite-cavity electrooptically tuned microchip laser represents an ideal solution for a high-sensitivity, high-tuning-rate, large-frequency-excursion solid state laser. The configuration, coupled with the simplicity, small size, robustness, high mode quality, and potential for low-cost mass production of the laser, should make it an attractive candidate for a large range of applications.

The electrooptically tuned microchip laser discussed here, illustrated in Figure 2-1, consists of a 0.5-mm-long piece of 1.8-wt% Nd:YAG bonded to a 1-mm-long piece of LiTaO₃. Both materials were polished flat and parallel on the two faces normal to the optic axis. The pump-side face of the Nd:YAG was coated dielectrically to transmit the pump light (810 nm) and to be highly reflective at the oscillating wavelength (1.064 μ m). The interface between the Nd:YAG and the LiTaO₃ was designed to be antireflecting at 1.064 μ m and to reflect the pump light, allowing double-pass absorption of the pump. The opposite face of the LiTaO₃ was coated for 2% transmission of the laser light. The LiTaO₃ was oriented with its c-axis orthogonal to the cavity axis. Electrodes were deposited on the two faces of the LiTaO₃ normal to the c-axis with an electrode spacing of ~ 1 mm.

In addition to being an electrooptic crystal, LiTaO₃ is piezoelectrically active. As a result, when a voltage is applied to the crystal both its physical dimensions and index are modulated. Normally, the change

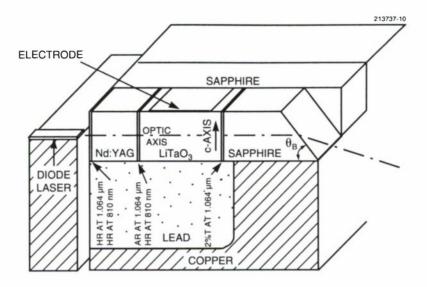


Figure 2-1. Cut-away illustration of a diode-pumped composite-cavity electrooptically tuned microchip laser showing the optical cavity and all materials used for acoustic damping. HR, highly reflecting; AR, antireflecting; T, transmitting; $\theta_{R'}$ Brewster's angle.

in dimensions has a small effect compared to the index modulation. However, a free-standing crystal can act as a high-Q acoustic cavity. At the resonant frequencies (which fall in the range from 500 kHz to several megahertz for the size crystal used), the piezoelectric effect can cause greatly enhanced frequency modulation of the laser. To eliminate these resonances, the LiTaO₃ was bonded to materials with the same acoustic impedance in order to transmit the electrically excited acoustic waves out of the crystal. In the two directions normal to the optic axis of the cavity we duplicated a proven technique [4]. Lead provided the electrical connection to the bottom electrode on the LiTaO₃ as well as impedance matching and damping for acoustic excitations propagating along the c-axis. Sapphire provided electrical insulation between the electrodes and acoustic impedance matching for excitations traveling along the a-axis (normal to the optic axis of the laser). Since sapphire does not damp the acoustic waves, these waves were further transmitted into copper. Grooves were cut into the copper and filled with polyimide to improve the acoustic damping.

Whereas in previous variations of electrooptically tuned Nd:YAG lasers acoustic damping was not required for waves propagating along the optic axis [4], in the composite-cavity microchip laser longitudinal acoustic resonances correspond to direct changes in cavity length and have a large effect on the tuning response. Since Nd:YAG is nearly impedance matched to LiTaO₃, acoustically the entire structure acts as a single crystal. To extract acoustic energy propagating along the optic axis of the cavity, sapphire was bonded to the output face of the device. Sapphire provides the needed transparency, electrical insulation, and acoustic impedance matching. The laser light exits the sapphire through a Brewster's-angle facet. This angled facet also reflects acoustic energy into the copper base, where it is dissipated.

The gain medium of the laser absorbs ~ 30% of the incident pump power from a butt-coupled laser diode and reaches threshold at an incident power of 100 mW. Despite spatial hole burning in the gain medium [6], the laser operates in a single longitudinal mode and polarization at output powers > 10 mW

(twice threshold). This is due to the short length of the cavity and the fact that the gain is localized near one of the end mirrors [7]. The device also operates in the lowest-order, nearly diffraction-limited transverse mode.

The free spectral range of the microchip cavity is 49 GHz. The presence of the birefringent LiTaO $_3$ in the cavity splits the polarization degeneracy of the cavity. The threshold for either polarization depends on how far the cavity mode for that polarization lies from the gain peak. Ideally, the cavity modes for the slowly tuned polarization (E-field perpendicular to the c-axis of the LiTaO $_3$) should straddle the gain peak. The more easily tuned polarization (E-field parallel to the c-axis) would then lie closer to the gain peak over most of the free spectral range of the cavity, allowing the maximum tuning range for single-mode operation in that polarization. We have obtained continuous tuning in a single mode without polarization switching over a range of 30 GHz.

To tune the frequency of the laser, a voltage is applied across the electrodes on the $LiTaO_3$. The $LiTaO_3$ fills a large portion of the cavity and provides a high tuning sensitivity. If we assume that all of the electric field generated by the electrodes is confined within the $LiTaO_3$, the calculated tuning response for the easily tuned polarization is 14 MHz/V, in good agreement with the observed value of ~ 12 MHz/V.

The tuning response of the composite-cavity electrooptically tuned microchip laser was measured out to 1.3 GHz. With acoustic damping only in the two directions orthogonal to the cavity axis, resonant enhancement of the tuning was observed at frequencies corresponding to the odd harmonics of the fundamental longitudinal acoustic resonance of the cavity along its optic axis (1.7 MHz), as shown in Figure 2-2. (With an equal number of expanded and contracted regions, the even harmonics do not

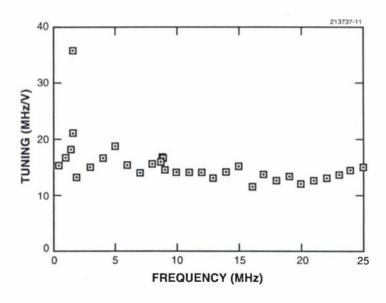


Figure 2-2. Tuning response of the composite-cavity electrooptically tuned microchip laser with acoustic damping only in the two directions orthogonal to the cavity axis. Resonant enhancement is observed at frequencies corresponding to the odd harmonics of the fundamental resonance of the cavity along its optic axis.

correspond to a net change in cavity length.) Below, between, and above these resonances, the laser tuned at ~ 12 MHz/V. We are currently repackaging the device with acoustic damping in all three directions, as discussed above. This should lead to a flat modulation response at rates from dc to several gigahertz.

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3. MATERIALS RESEARCH

3.1 MOLECULAR BEAM EPITAXY GROWTH OF HIGH-MOBILITY n-GaSb

The molecular beam epitaxy (MBE) growth of GaSb and its alloys is receiving increasing attention as a means of preparing multilayer structures for a variety of device applications, including diode lasers, photodetectors, and heterojunction transistors. Despite this increasing attention, much of the observed experimental data on the transport properties of GaSb falls short of what is expected from theoretical considerations, especially in comparison to more fully explored compound semiconductors such as GaAs. For example, as has been known for many years, theoretical calculations show that the lattice-limited electron mobility in GaSb should exceed that of GaAs, yet until the present work the measured electron mobilities in GaSb have not even approached those observed in GaAs at similar carrier concentrations. One important consideration in understanding the experimentally observed electrical properties of n-type GaSb is the presence of an unusually large (10^{16} – 10^{17} cm⁻³) native acceptor background that occurs in nominally undoped material. Although the exact details of this native acceptor are not yet fully understood, the concentration has been found to depend on both growth technique and growth conditions [1] and is generally attributed to an antisite defect or defect complex [2]. We have now demonstrated that reproducible background acceptor levels of $\sim 1 \times 10^{16}$ cm⁻³ can be obtained by MBE, and with such low background levels, high-quality, lightly doped n-type material can also be obtained.

The GaSb epilayers in this study were grown in a commercial MBE system using Ga (99.99999%) and uncracked Sb (99.9999%) sources. The GaSb layers for Hall measurements were grown on (100) semi-insulating GaAs substrates prepared with an H_2SO_4 -based etch, and layers for capacitance-voltage (C-V) and photoluminescence measurements were grown on (100) n-GaSb substrates (Te doped ~ 4 × 10^{17} cm⁻³) prepared with a Br_2 -based etch. To grow n-type GaSb epilayers, a GaTe (99.9995%) dopant source was used [3], while to grow intentionally p-type GaSb, required to form p-n junctions for C-V samples, a Be dopant source was employed. Growth rates for GaSb of ~1 μ m/h were used, and sample thicknesses were sufficient to minimize surface and interface effects. We optimized both the III/V ratio and the substrate temperature for the growth of GaSb. The GaSb epilayers grown under optimized conditions showed smooth and specular surface morphologies on GaSb substrates and only a slight surface texture on GaAs substrates. To perform the Hall measurements, we used etched cloverleaf structures for the van der Pauw technique, with ohmic contacts provided by alloyed Sn and In/Sn metallic dots. The C-V samples were fabricated with mesa-etched diodes and similar alloyed contacts.

As a first step in this study we intentionally grew a number of nominally undoped GaSb epilayers under a wide variety of growth conditions and performed Hall measurements on these samples. As was expected, all samples showed p-type conduction. What was unexpected, however, was the observation of relatively small variation of the mobility and apparent background acceptor concentration. Varying the Sb₄/Ga beam equivalent pressure (BEP) ratio from 3:1 to 10:1 and changing the substrate temperature T_s from 490 to 530°C had little effect. Only by increasing the substrate temperature to > 550°C did we see any significant variation in the Hall results for these p-type samples. When we repeated the growth of p-type samples using exactly the same growth conditions, we saw < 10% variation in the 300-K p-type

background ($\sim 1.1 \times 10^{16} \text{ cm}^{-3}$ with mobilities $\sim 820 \text{ cm}^2/\text{V s}$) and somewhat more variation in the measured 77-K background ($\sim 2.4 \times 10^{15} \text{ cm}^{-3}$ with mobilities $\sim 4100 \text{ cm}^2/\text{V s}$).

After obtaining these encouraging results on the reproducibility of the p-type background, we grew a number of n-type samples on GaAs substrates under various conditions. These samples were doped with Te from the GaTe source at a donor density N_D exceeding the background acceptor defect density N_A , to give a conduction electron concentration $n = (N_D - N_A)$. The effect of the growth conditions on the Hall results was found to be greater for the n-type samples than for the p-type ones. An Sb₄/Ga BEP ratio of ~5:1 and a substrate temperature of ~515°C gave the highest mobility for a given electron concentration. The data for μ vs n are plotted in Figure 3-1, along with the best previously reported data for GaSb layers on GaAs substrates, which were grown by MBE with a SnTe dopant source [4]. Figure 3-1 also shows some previous data for undoped n-GaSb grown by liquid phase epitaxy (LPE) on GaSb, where the substrate was mechanically removed in order to perform the Hall measurement [5]. Our highest values of μ_{300} and μ_{77} are 7.6×10^3 and 1.3×10^4 cm²/V s, respectively, which were obtained for a sample with n_{300} and n_{77} of 1.2×10^{16} and 2.0×10^{16} cm⁻³, respectively. The μ_{300} value is about 50% higher than the values given in literature summaries for the peak electron mobility in GaSb at room temperature, and exceeds by about the same amount the highest values of μ_{300} reported [4] for n-GaSb deposited on GaAs substrates. The highest value of μ_{300} that has been reported for n-GaSb is 7.7×10^3 cm²/V s, which was measured for a sample with $n_{300} = 3.5 \times 10^{15}$ cm⁻³ that was grown by LPE on a GaSb substrate [5]. This mobility value seems questionable, however, since the μ_{300} values measured in the same study for samples with $n_{300} = 8 \times 10^{15}$ and 7×10^{15} cm⁻³ were only about 3×10^3 cm²/V s.

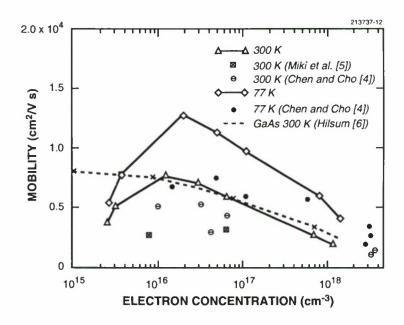


Figure 3-1. Mobility vs n-type carrier concentration of GaSb at 300 and 77 K.

Figure 3-1 also shows the curve of μ_{300} vs n_{300} published by Hilsum [6] as an empirical fit to the highest mobility values for n-GaAs reported in the literature. For values of n_{300} exceeding 10^{16} cm⁻³, our values of μ_{300} for n-GaSb are comparable to the GaAs values. For values of n_{300} in the low 10^{16} cm⁻³ range, the GaSb mobility values are actually somewhat higher, even though the GaSb samples are significantly compensated by the native acceptor defects, while the GaAs samples are essentially uncompensated.

Since the background acceptor concentration N_A in our Te-doped n-GaSb samples is about 10^{16} cm⁻³, all of these samples have $(N_D + N_A)$ values exceeding this level. For such high concentrations of charged centers, ionized impurity scattering is expected to be the principal carrier scattering mechanism at both 77 and 300 K. The data of Figure 3-1 are qualitatively consistent with ionized impurity scattering. For all the samples, μ increases when the temperature is decreased from 300 to 77 K, although the increase is much smaller than predicted by the $T^{-5/2}$ dependence characteristic of ionized impurity scattering. For samples with $n > 1 \times 10^{16}$ cm⁻³, μ increases as $n = (N_D - N_A)$ decreases, as expected because of the associated decrease in the concentration of scattering centers $(N_D + N_A)$. When n is decreased below 10^{16} cm⁻³, however, μ decreases sharply. This decrease in μ , which has also been observed for n-InSb, can be attributed to the reduction in the electrostatic screening of the charged scattering centers that occurs because of the decrease in electron concentration. The screening also is lowered with decreasing electron concentration at the higher concentration levels, but in that range the reduction in $(N_D + N_A)$ is sufficient to cause the observed increase in mobility. In the lower concentration range, since N_A is essentially constant and N_D is less than N_A , the reduction in $(N_D + N_A)$ is too small to overcome the effect of reduced screening.

As a confirmation of the capability of GaTe to be used as a dopant source of Te for growing high-quality n-GaSb over a wide range of donor concentrations, Figure 3-2 shows an Arrhenius plot of the

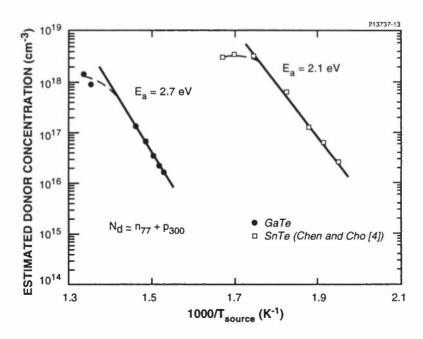


Figure 3-2. Arrhenius plot of estimated donor concentration vs source temperature for GaTe and SnTe sources.

estimated donor concentration as a function of GaTe source temperature, with added data from Chen and Cho [4] on SnTe. To provide an estimate of the actual donor concentration for this plot we have used the method of Chen and Cho [4]. Their method addresses the complication in interpreting Hall measurements in the light of the two-band model for electron conduction in GaSb, where the energy separation is relatively small (~ 0.08 eV at 300 K) between the high-mobility Γ conduction band valley and the low-mobility L valley. In the Chen and Cho method, since the total electron concentration is approximately given by the Hall concentration at low temperatures (when intervalley transfer is less likely), the estimated donor concentration is given by the low-temperature Hall concentration plus the room-temperature background acceptor concentration. Relative to SnTe the results for GaTe show a higher activation energy but a similar saturation level near 2×10^{18} cm⁻³.

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4. SUBMICROMETER TECHNOLOGY

4.1 COMPARISON OF ETCHING TOOLS FOR RESIST PATTERN TRANSFER

Multilayer and surface imaging resist techniques as alternatives to conventional single-layer resist processing may become essential in optical lithography at 0.25- μ m resolution and below. These techniques use a carbon-based planarizing layer to overcome depth-of-focus limitations associated with the short wavelength and high numerical aperture necessary for high-resolution patterning. The pattern is imaged near the resist surface, and dry anisotropic etching is used to transfer the pattern through the planarizing layer. The pattern transfer requirements for a production-worthy resist system are quite severe. Sub-0.5- μ m geometries must be transferred without linewidth loss at rates compatible with single-wafer processing (~ 1 μ m/min). Additionally, the resist profiles must exhibit high anisotropy, without residue formation. Last, the tool of choice should be able to etch these small features uniformly over an 8- or even 12-in.-diam wafer.

A positive-tone silylation resist scheme [1] was used to evaluate a conventional reactive ion etching (RIE) tool as well as high-density plasma systems including a magnetically enhanced reactive ion ctching (MERIE) tool, an electron cyclotron resonance (ECR) reactor, and a helical resonator reactor, The silylation resist process used in this study starts with a polyvinylphenol (PVP) resin that is crosslinked by exposure to 193-nm light. Next, the sample is exposed to a silicon-containing vapor (dimethylsilyldimethylamine) at a temperature of 100° C and a pressure of 10 Torr for 1 min. The unexposed areas incorporate silicon, whereas the exposed areas do not. The sample is then subjected to an oxygen plasma, and the areas containing silicon are converted to a SiO_x compound that acts as an excellent etch mask to the oxygen plasma. The exposed areas containing little or no silicon are etched, resulting in a positive-tone resist pattern. The silylation conditions listed above were optimized for the PVP resin and the parallel-plate RIE tool described below.

A conventional parallel-plate RIE tool with a roots blower pumping package was used in this study. The flow rate in the system was held constant at 10 sccm, which resulted in a processing pressure of 25–35 mTorr. The self-bias was held constant at -230 V by applying 60 W of RF power, and the wafer was not cooled during etching.

The magnetic field in the MERIE tool was adjusted to achieve maximum uniformity for 3-in, wafers. The gas flow was 40 sccm of O_2 , the pressure was 2.1 mTorr, and the temperature during etching was fixed at 0°C. The RF power was adjusted from 300 to 1000 W to yield a self-bias between -33 and -65 V.

The beam-type ECR source operated between 700 and 1000 W of microwave power and was pumped by a 1000-L/s turbomolecular pump. The N_2O and O_2 processing gases were introduced into the source at a rate of 40 sccm. A separate RF power supply, connected to the wafer platen, was adjusted from 5 to 30 W to yield a self-bias between -9 and -80 V. The pressure was fixed at 1.3 mTorr, and the temperature during etching was held at 5°C.

The helical resonator reactor was operated at 2000–2500 W of RF power in the source. As with the ECR system, self-bias was established by independently powering the wafer chuck. The RF power to the chuck was varied from 50 to 125 W, resulting in bias voltages ranging from -10 to -150 V depending on other parameters such as gas flow and pressure. This system is pumped by two 400-L/s turbomolecular pumps. The oxygen flow rate was varied from 50 to 200 sccm, and the wafer was backside cooled with He to -40° C at the start of each etch run.

At the flow rates and pressures used in our conventional RIE tool, a high (> 200 V) self-bias is necessary to achieve straight sidewalls. Under these conditions, etch rates of only 80 nm/min are typical, and this is far too slow for practical single-wafer processing. In addition, dry development of silylation resist under high self-bias conditions results in the formation of residue in open field areas [2]. The observed residue, which has been attributed to redeposition of sputtered mask material, is a function of feature size for periodic structures. For high aspect ratio features, the sputtered material is redeposited only on the sidewalls, so that significant residue is observed only in open areas. High ion density sources can provide much higher etch rates at lower self-bias voltages. The lower self-bias reduces sputtering of the mask and thus leads to little or no residue formation. In our study, residue could be completely eliminated for all the sources except the conventional RIE.

Focus and exposure latitudes were investigated for the four different etching tools using the silylation resist system. Figure 4-1 illustrates total exposure latitude plotted as a function of feature size for one representative sample from each etching tool. In all cases the etched features had vertical sidewalls. The total exposure latitude represents the range in exposure dose where $\pm 10\%$ linewidth was maintained for a nominally equal line and space grating structure. The lithographic k_1 factor is given on the upper abscissa. For features printed at k_1 values > 0.4, the three high-density sources show slightly better process latitude than the RIE tool, presumably due to slightly better selectivities achieved with these tools. Focus latitude was comparable for all tools and was as high as $\pm 4~\mu m$ at k_1 values of 0.5. The relatively large depth of focus is attributable in part to the low numerical aperture (0.22) of our stepper.

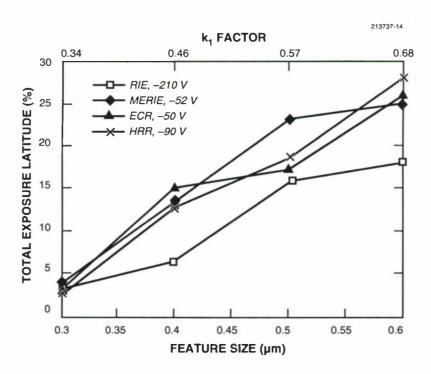


Figure 4-1. Plot of total exposure latitude as a function of feature size for representative silylation samples etched with RIE, MERIE, ECR, and helical resonator reactor (HRR) etch tools. The k_1 factor for our exposure tool is also shown.

In addition to focus and exposure latitude, etching uniformity was also investigated on three of the tools, and the results are summarized in Figure 4-2. In this figure, the standard deviation (1σ) of the space-to-period ratio is plotted as a function of feature size. For the MERIE and RIE tools, the calculations were made using 5 dies placed in a star pattern on 3-in. wafers and evaluating the etch uniformity over the central 2.5 in. of the wafer. The same features were measured on every die. For the helical resonator reactor tool, 5- and 6-in. wafers were used. For the sample run at a lower self-bias voltage, the star pattern just described was used with a 5-in. wafer, yielding uniformity over the central 4 in. of the wafer. The sample run at -70-V bias was a 6-in. wafer exposed with an extended star pattern. This arrangement enabled the measurement of 17 dies over the central 4 in. of the wafer. Except for the low-bias helical resonator reactor sample, the linewidth nonuniformity on the tools was < 4%.

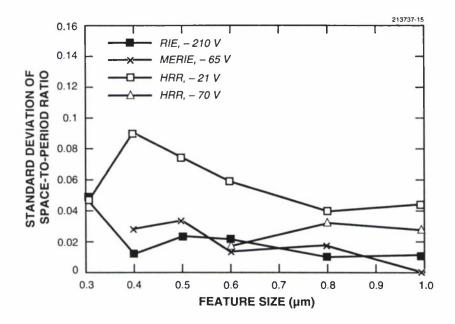


Figure 4-2. Linewidth uniformity measured using the standard deviation of the space-to-period ratio as a function of feature size for silylation samples etched with RIE, MERIE, and helical resonator reactor etch tools.

All the etching systems examined in this study show good process latitude, straight sidewalls, and high etch uniformity over 3-in. wafers. The high-density sources can achieve high etch rates without compromising the etch profiles or depositing residue on the substrate. Figure 4-3 illustrates the profiles of a silylation resist system etched with ECR, MERIE, and helical resonator reactor tools under optimized conditions. Although similar profiles are attainable using RIE, the low etch rate and formation of residue make it inadequate for use in a production environment. The MERIE tool has the advantage of extensive

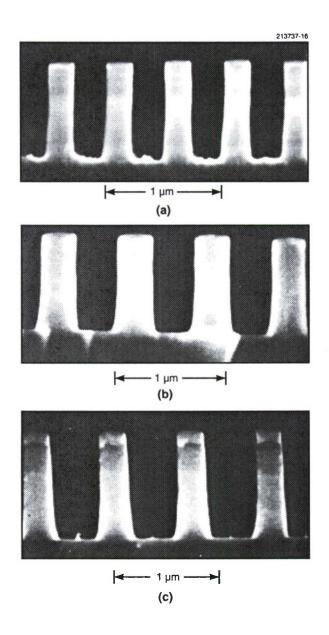


Figure 4-3. Scanning electron micrographs showing profiles of silylated resists etched using (a) the ECR etch tool operated at 700 W, -75-V bias, and an etch rate of 240 nm/min; (b) the MERIE etch tool operated at 1000 W, -65-V bias, and an etch rate of 650 nm/min; and (c) the helical resonator reactor etch tool operated at 2500 W, -90-V bias, and an etch rate of 950 nm/min.

testing in a manufacturing environment [3], but ECR and the helical resonator reactor have more flexibility than MERIE for controlling etch rate, profile, and uniformity, because the ion flux can be decoupled from the ion bombardment energy.

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4.2 VERTICAL MOSFETS FOR HIGH-DENSITY MEMORIES

A vertical metal oxide semiconductor field-effect transistor (MOSFET) device structure is being developed that should be suitable for fabricating an ultradense transistor array for read-only memory (ROM) and programmable read-only memory (PROM) applications. The goal is to construct a solid state ROM/PROM integrated circuit (IC) with storage capacity comparable to a compact disk read-only memory (CDROM) but with much higher bit density and a much faster access time. This IC would be applicable to high-performance and portable computer systems.

Current CDROM technology provides approximately 5×10^9 bits of storage on a 12-cm-diam disk. Implementing this much storage on a chip of 2-cm² area will require a memory cell pitch of 0.2 μ m, which implies the use of advanced lithographic tools and an area-efficient memory structure. Figure 4-4(a) shows an *n*-channel vertical MOSFET topology that should be useful in achieving this goal, and Figure 4-4(b) shows this device in a memory array. The silicon substrate provides the source contact for all the transistors in the array. Individual drain contacts are fabricated on the tops of the cylindrical devices, and the gate oxide and gate encircle the structure. Scaling this vertical MOSFET structure to achieve greater device density does not require scaling the gate length, so many of the short-channel device effects experienced with scaling in the conventional planar MOSFET structure are avoided.

Stacking the source and drain contacts minimizes the device area in the vertical MOSFET, but in this topology the p-type body of the transistor is electrically floating between the n^+ drain on the top and the n^+ source on the bottom. A similar situation exists for silicon-on-insulator (SOI) devices and is termed the floating-body effect. During operation in the ON state, high electric fields at the body/drain junction can lead to impact ionization. At drain biases greater than a few volts the impact-generated holes can charge the floating body to the point where the source/body junction becomes forward biased, resulting in an increase in the drain current. This bipolar action is responsible for the so-called kink effect reported in many SOI devices. One solution to this problem for the vertical MOSFET involves an annular source connection that provides a conducting channel between the substrate and the body of the device. This approach has been used in the surrounding-gate transistor [4], but the lateral extent of the source connection would limit the packing density in memory array applications. We have chosen to adjust the source and drain doping to minimize the effects of the floating body. A lightly doped drain structure is used to reduce the electric fields in the drain region, thereby decreasing impact ionization. In addition, a lightly doped source structure is used to reduce the emitter efficiency of the parasitic bipolar transistor.

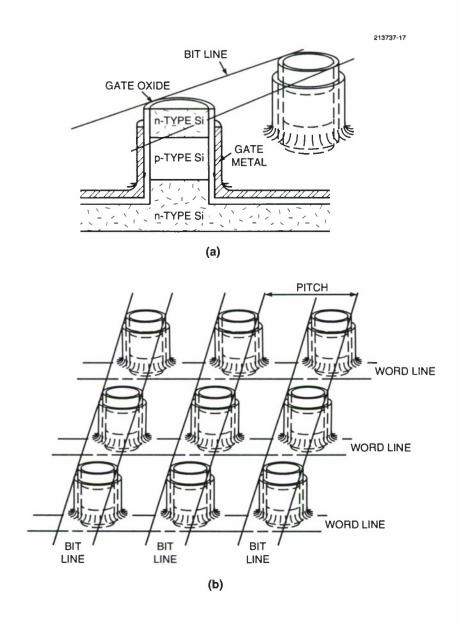


Figure 4-4. (a) Cross section of the vertical MOSFET structure, and (b) schematic representation of this structure used in a ROM/PROM array.

Since the entire wafer substrate serves as a common source contact, the added resistance from the lightly doped source does not present a problem for the dense ROM/PROM array.

The vertical MOSFET process flow requires four lithographic masking steps and makes extensive use of standard silicon process modules. The first mask defines the transistor locations which are formed using a silicon trench etch technology, the second defines the polysilicon gate (word line), the third defines the contact locations, and the fourth defines the metal (bit line). Of these four masks the third represents the most critical alignment step. Future enhancements to the process flow will incorporate a self-aligned contact process utilizing a chemical-mechanical planarization technique and a voltage-programmable link structure.

Measurements of the first n-channel devices (2- μ m diameter, 1- μ m channel length) show excellent electrical characteristics with no sign of the kink effect. These first devices can be operated with a source-to-drain voltage $V_{\rm DS} > 15$ V and with an off-state drain current $I_D < 10$ pA at $V_{\rm DS} = 5$ V. The 20-nm-thick gate oxide surrounding the vertical transistor structure withstands a gate voltage $V_{\rm GS} > 10$ V at $V_{\rm DS} = 0$ V without breaking down. The threshold voltage $V_{\rm TH}$ is 0.2 V with a subthreshold slope of 80 mV/decade. The $V_{\rm TH}$ is lower than the design value of 0.5 V and will be corrected in future runs by adjusting the transistor body doping. Figure 4-5 shows an I_D vs $V_{\rm DS}$ plot with $V_{\rm GS}$ as a parameter for a typical 2- μ m-diam vertical MOSFET.

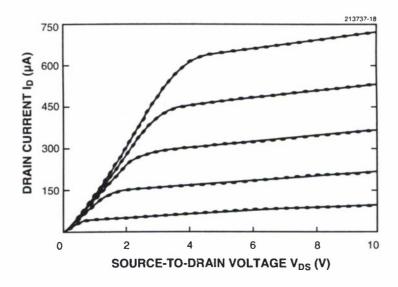


Figure 4-5. Measured I_D vs V_{DS} with V_{GS} as a parameter for a 2- μ m-diam, 1- μ m-channel-length, n-channel vertical MOSFET.

The p-channel device offers another solution to the kink effect problem. The reduced mobility of the holes in these devices reduces the impact ionization at the drain of the transistor and thereby reduces the kink effect. The fabrication and electrical characterization of the first p-channel vertical transistor run have recently been completed. The devices exhibit normal characteristics with no sign of the kink effect.

Thus far, all devices and simple ROM arrays have utilized $1 \times$ optical lithography, which has limited contact cut resolution to $1 \mu m$. We are developing a combined optical and electron-beam lithography process to pattern 0.2- μm contact cuts on 0.5- μm -diam vertical MOSFET devices. Recently an i-line reticle set incorporating vertical transistor test structures and memory arrays has been designed. The i-line capability will allow routine patterning of 0.6- μm geometries over large field sizes.

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5. HIGH SPEED ELECTRONICS

5.1 ANALYSIS OF FIELD-EMISSION CONES USING HIGH-RESOLUTION TRANSMISSION ELECTRON MICROSCOPY

A classic approach by the vacuum microelectronics community for making field-emission cathodes is to fabricate arrays of molybdenum cones having sharp tips with radii ≤ 20 nm [1],[2]. Arrays of such cones have demonstrated useful levels of emission current, but typically only 25% of the tips provide the majority of the current. In addition, conventional scanning electron micrographs indicate that the effective emission area of these tips should be ≥ 10 nm², whereas an analysis of experimental emission data indicates that the area is only 0.1-0.5 nm². To the present the reasons for the nonuniformity and the discrepancy in emission area have been little understood.

In an endeavor to explain these phenomena better, we have recently used a high-resolution transmission electron microscope (TEM) to study the detailed structure of the tips of molybdenum field-emission cones. This microscope is capable of crystal-lattice imaging and has much finer resolution capability than any scanning electron microscope used to study these structures in the past. Our experimental geometry is shown in Figure 5-1. A small sample is cleaved from an array of molybdenum cones on a silicon wafer and mounted on the copper sample-holder ring of our TEM at a glancing angle to the electron beam. Through careful sample positioning we are able to study the end sections of the cones individually.

Figure 5-2 shows a TEM micrograph of an end section of a typical cone. The main feature of note is that the tip has a somewhat irregular shape, with one primary protrusion and a sharp secondary protrusion ~ 4 nm below it. The radius of each protrusion is ~ 1 nm. The average size of the grains in this polycrystalline sample is ~ 5 nm, and it is probably these grains that cause the sharp protrusions. Although not evident in Figure 5-2, we observe faint, closely spaced striations near the tip, which are a lattice image of one grain, and larger periodic striations ~ 50 nm from the tip, which are diffraction interference patterns caused by the passage of the beam through two grains. Also detectable in the original micrograph of Figure 5-2 is a thin (< 1 nm) amorphous surface layer. At the present time we are unsure as to its origin. The layer was perhaps introduced during the processing of the sample for TEM analysis. X-ray photoelectron spectroscopy was performed on a portion of the sample that was not prepared for TEM analysis, and the surface layer was found to consist of MoO_3 and carbon.

The structure shown in Figure 5-2 offers an explanation for the phenomena cited above. The electric field on the surface of the tip during an emission experiment will be strongly enhanced on the point of a protrusion like the primary one observed. This local field enhancement together with the small size of the protrusion would give a very small emission area entirely consistent with that observed. Furthermore, significant variation exists in the structure of the protrusions from tip to tip—some tips have a very sharp primary protrusion while others have a more blunt shape that would produce less field enhancement. This variation together with the presence of the surface oxide layer explains why many tips

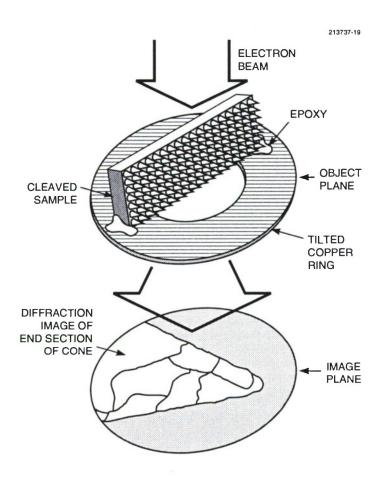


Figure 5-1. Experimental geometry for TEM analysis of field-emitter cones. Through careful positioning, single cones can be studied individually.

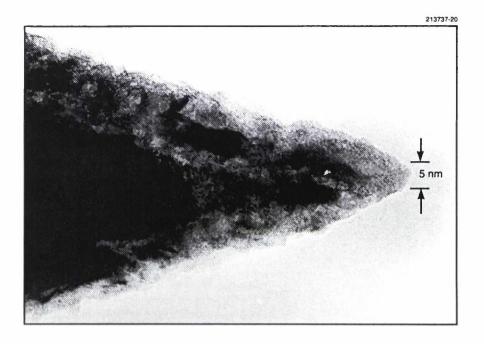


Figure 5-2. TEM of the end section of a molybdenum field-emitter cone. The radius at the tip is ~ 1 nm.

in an array do not emit current while others do. We are applying the knowledge gained in these TEM studies to optimize the emission from arrays of these field-emitter cones.

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6. MICROELECTRONICS

6.1 CALCULATIONS OF CCD CHARGE-TRANSFER INEFFICIENCY VS PACKET SIZE

In a previous report we described measurements of charge-transfer inefficiency (CTI) as a function of charge-packet size in a buried-channel charge-coupled device (CCD) [1]. The data were obtained on a device that had been irradiated with 40-MeV protons in order to study the effects of displacement damage created by energetic particles in a space environment. For minimal charge trapping, the device has a narrow potential trough along the center of the channel to reduce small packets to the least volume [2],[3]. In this report, we describe the results of numerical simulations that explain the major features of the experimental data.

Figure 6-1(a) illustrates a cross section through a pixel of the CCD structure (the direction of charge transfer is normal to the page) and defines the coordinate system used later. The boundaries of the channel are set by thick field oxide at the channel sides, with electrons confined to a region beneath the thin oxide containing a buried channel. The buried channel consists of an implant that is uniform across the channel width plus an additional implant in the form of a narrow (2 μ m) stripe down the channel center. The latter creates a region of deeper potential, or a potential trough, that constrains small charge packets to a smaller volume than would be the case without the trough. The uniform buried channel and trough implant doses are each 4 \times 10¹¹ cm⁻² (phosphorus), resulting in a trough potential about 1.5 V deeper than in the adjacent nontrough region.

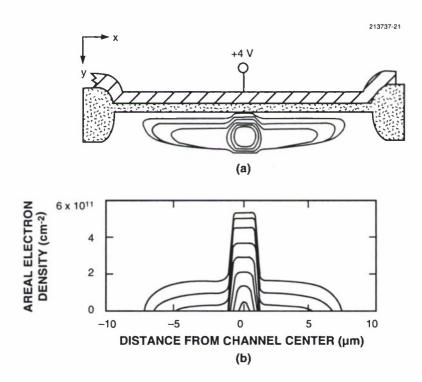


Figure 6-1. (a) Cross-section of a CCD channel with a 2-µm-wide implant in the center to confine small charge packets. The curves depict outlines of charge packets corresponding to a sequence of electron quasi-Fermi potentials. (b) Areal electron density vs distance from the channel, obtained by integrating the electron concentration with depth (y-direction).

The results of two-dimensional simulations of the electron distribution in the buried channel are illustrated in Figure 6-1. Figure 6-1(a) shows the outlines of a series of charge packets of different sizes corresponding to a sequence of quasi-Fermi potentials. The boundaries of the charge packets are chosen as the points at which the electron concentration is 1% of its peak value at the center of the channel. Figure 6-1(b) was obtained by integrating the electron concentration with depth (along the y-direction) to obtain the net areal electron density as a function of distance from the channel center. The calculations show that small quantities of charge are confined to the trough, but as the packet grows the trough is eventually filled and the excess charge resides in the nontrough portion of the channel.

The premise behind the use of the trough is that charge-trapping effects can be minimized by reducing the volume of a charge packet. If the traps are uniformly distributed within the buried channel, the carrier loss per transfer, ΔN , will be proportional to the charge-packet volume $V_{\rm cp}$, and the CTI per transfer can thus be written

$$CTI = \frac{\Delta N}{N} = K \frac{V_{\text{cp}}}{N} , \qquad (6.1)$$

where N is the number of carriers in the packet and K is a constant involving, among other things, the volume density of traps. To compute $V_{\rm cp}$ and N requires a simulation in three dimensions. Since such a program was not available to us, we devised an approximate method of calculating these quantities using results from the two-dimensional simulation program CANDE, which was also employed to obtain the results in Figure 6-1.

To calculate $V_{\rm cp}$ and N we need to know the charge density and packet shape in the third, or z, dimension. We can approximate these quantities by simulating the CCD in the y-z plane (the plane defined by the direction of charge transfer and the direction normal to the device surface). In this plane the outlines of the charge packets are a series of nested oval shapes (for a series of quasi-Fermi potentials), each characterized by an area A and a maximum height H in the y-direction at x = 0. To calculate $V_{\rm cp}$ we take the packet outline computed in Figure 6-1 for the x-y plane and use the results from the y-z simulations to estimate its three-dimensional shape. Figure 6-2 illustrates the basic step in the volume computation. At each x_i the packet in the x-y plane has a height H_i , and we attach to this curve the y-z curve that has $H = H_i$ and corresponding area A_i . We thus create a family of curves that define the packet surface. The volume is computed by summing contributions of the form $(x_{i+1} - x_i)(A_{i+1} + A_i)/2$ for all i.

The method for calculating N involves first generating a set of curves in the y-z plane of areal electron density vs z [similar to those in Figure 6-1(b) for the x-y plane] as well as the integral over z of each curve, which gives the total carrier count n_p in this plane in units of cm⁻¹. For each curve there is a maximum areal density n_{max} at the center of the well (z = 0). To compute the total carrier count N in a packet we use the integrated areal density curve for the packet in the x-y plane (z = 0). For each density value n_i at a point x_i on this curve we find the curve in the y-z plane whose $n_{\text{max}} = n_i$, and we replace n_i with the carrier count n_p of the y-z curve. The total carrier count is then the sum of contributions of the form $(x_{i+1} - x_i)(n_{p,i+1} + n_{p,i})/2$.

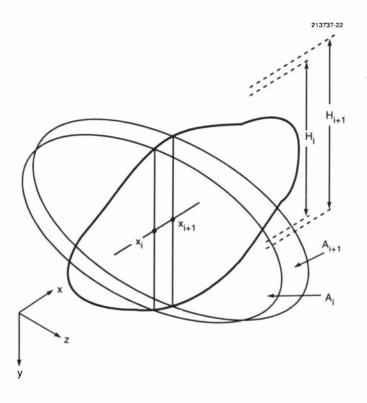


Figure 6-2. Illustration of the computation of charge-packet volume using two-dimensional simulations of packet outlines from the x-y and y-z planes.

Figure 6-3 shows the CTI vs N at $T=-115^{\circ}\mathrm{C}$ reported earlier [1]. In the same figure is a curve of $KV_{\rm cp}/N$ vs N computed with the methods just described and with K selected to bring the calculated curve into best agreement with the simulated results. The calculated curve extends down to $N\approx 500~e^-$, below which the computations became unreliable because the simulation grid used was too coarse in relation to the packet size. From 500 to 30000 e^- the calculation agrees well with the experiment. It also confirms that the trough is filled at approximately 30000 e^- , leading to an abrupt increase in CTI for larger N. However, the calculated curve somewhat overestimates the CTI in the latter regime. Nevertheless, the computation method described here appears to be a useful tool in predicting the relative CTI of CCDs over a wide range of packet sizes.

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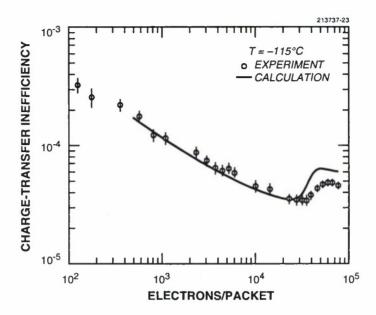


Figure 6-3. Experimental and calculated curves of CTI vs packet size on a proton-irradiated device. The calculation was based on an approximate method of computing the volume and carrier count in a packet, as described in the text.

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7. ANALOG DEVICE TECHNOLOGY

7.1 SHIFT REGISTER FROM SINGLE-FLUX-QUANTUM LOGIC

Single-flux-quantum (SFQ) logic, as presented by Likharev and Semenov [1], represents a third attempt to produce a technologically viable electronics out of superconductivity. The first two attempts, the cryotron and latching Josephson logic, failed to motivate designers to abandon standard technology, even in niche applications, in part because of speed limitations. In contrast, SFQ logic can, in theory, be pushed to frequencies of 100 GHz and beyond. This fact explains the recent explosion of work in this topic at SUNY Stony Brook, NIST, Hypres, and Lincoln Laboratory.

The general principle behind SFQ logic is that an overdamped Josephson junction, displaying a nonhysteretic current-voltage (I-V) curve, can be made to generate a single, narrow voltage pulse [2]. It is this pulse that creates the fixed-size propagating signals that run through the circuit. Moreover, because of the quantum nature of superconductivity, these voltage pulses can be thought of equally well as single magnetic flux quanta moving through the circuit, and hence the logic family's name.

As an initial demonstration of the SFQ principles using Lincoln Laboratory's lithographic capability, we have recently fabricated a nine-cell linear SFQ shift register using a dual-dielectric selective niobium anodization process [3]. This circuit, a schematic of which is shown in Figure 7-1, is essentially a linear array of shunted Josephson junctions connected in parallel with a series inductance between each junction. The voltage sources provide a two-phase clock, whereby pulses of current are sent down alternating Josephson junctions. Since the clock current is purposely made close to the maximum that each junction can handle before switching to the V > 0 state, a simultaneous perturbing current introduced by the third voltage source (V_{IN}) is enough to switch the first junction into this state. As a result current is diverted through the inductor and the second junction, thus introducing a flux quantum into the first cell. This circulating current persists in the first cell, even after the first clock and input are brought to zero, until the second clock biases the second junction. Now, the circulating current is enough to cause the second Josephson junction to switch, and so the flux quantum moves to the second cell. In this way, a flux quantum (representing a logic bit 1) is moved along the shift register. In contrast, if the first cell contained no circulating current, then the second cell would receive the logic bit 0.

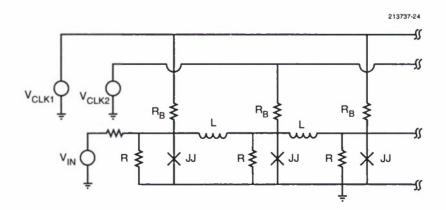


Figure 7-1. Schematic of a single-flux-quantum shift register.

Figure 7-2 shows a micrograph of the fabricated circuit along with some test results made at quasistatic (10 kHz) speeds. Notice that a flux quantum does not appear at the latching gate at the end of the shift register until it has passed through all nine cells. When packaged appropriately, our device has successfully operated at frequencies of 100 MHz.

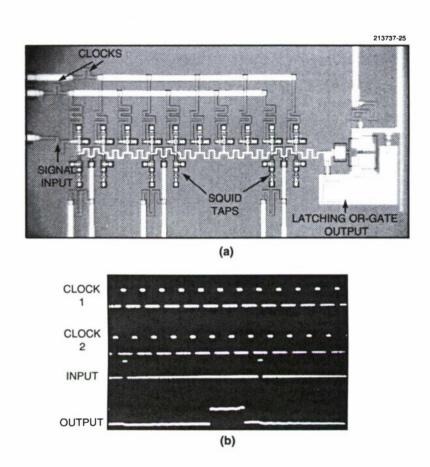


Figure 7-2. (a) Micrograph of a fabricated shift register, and (b) circuit test results at quasistatic speeds.

To make the junction switch as rapidly as possible (and thus provide the maximum logic speed), the critical current of the junction must be made as large as possible. The trade-off, however, is that if the junction critical current is too large, the device will become underdamped and yield multiple voltage pulses when it is switched. Estimates [1] show that for a practical lithographic junction size $\sim 0.25 \ \mu m^2$ the critical current density should be $\sim 50 \ kA/cm^2$. Although the lithography issues for this requirement are not trivial, fabrication processes do exist. Both the dual-dielectric selective niobium anodization process developed at Lincoln Laboratory and the planarized all-refractory technology for superconductors

developed at IBM and currently being implemented at Lincoln show promise in obtaining the necessary linewidths. However, the reliable attainment of ultrahigh critical currents, which involves problematic theoretical and experimental issues, remains a considerable challenge. Present technology typically limits the critical current to < 5 kA/cm² in high-quality junctions. At Lincoln Laboratory, we have developed a program, in collaboration with AT&T and IBM through the Consortium for Superconducting Electronics, to boost the level of critical current densities in junctions in a manner suitable for large-scale lithography. Presently, the best high-quality junctions made at Lincoln, ~ 17 kA/cm², represent the state of the art. We expect to push this limit higher soon.

Because of its relatively simple nature, a parallel combination of unshunted Josephson junctions represents an ideal testbed for developing both design rules and on-chip diagnostics. For example, the Fiske modes, representing the resonance of a flux quantum bouncing back and forth along the line, provide an accurate means to measure the inductance of each cell in the circuit [4]. We have also used superconducting quantum interference devices and transformers to magnetically couple into the individual cells. In this way, it is possible to actually observe the passing of the flux quantum as it propagates down the line. Through the use of these diagnostics and on-chip clocking, we hope to demonstrate much higher frequencies of operation without a sophisticated measuring apparatus.

K. A. Delin

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This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period I August through 31 October 1992. The topics covered are Electrooptical Devices, Quantum Electronics, Materials Research, Submicrometer Technology, High Speed Electronics, Microelectronics, and Analog Device Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, DARPA, Navy, SDIO, and NASA.

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